

respectfully requested in view of the amendments and following remarks.

Interview

The cooperation and courtesy extended by Examiner Dinh and Examiner Paladini during the personal interview with Applicants' representative, Hong Xu, on October 7, 2002 is noted with appreciation. A copy of Summary of Interview is also attached as an appendix with this Response.

Drawings

Five sheets of drawings were filed initially with this application. However, the Office Action does not indicate whether these drawings are acceptable. Applicants respectfully request the indication of acceptability during the next official communication from the U.S. Patent and Trademark Office.

Summary of Amendments

The specification is amended to more closely conform with U.S. practice.

Claims 1-5, 7, 9-14, 16-17, 21-23, 25-27 and 31-32 are amended to address all but one 35 U.S.C. §112 rejections made in the Office Action. The 35 U.S.C. §112 rejection of Claim 15, made on page 3 of the Office Action, is respectfully traversed.

Claim 20 is canceled and its subject matter is added to claim 17. Therefore, no new matter is added to claim 17.

Summary of the Office Action

The Office Action makes numerous 35 U.S.C. §112 rejections of Claims 1-5, 7, 9-17, 20-23, 25-27 and 31-32.

Claims 17-23 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,294,744 (“KINOSHITA”). The Office Action states that Figs 3D-3F of KINOSHITA disclose a roughened inner wall being covered with a roughened electroless plating layer.

Claims 1-16 and 24 are rejected under 35 U.S.C. §103(a) as being obvious over KINOSHITA. The Office Action alleges that KINOSHITA shows, citing column 4, lines 59-61, that its viahole has a diameter of less than 25 micrometers. The Office Action admits that KINOSHITA does not teach a thickness of its conductor circuitry layer being less than a half of the viahole diameter. But the Office Action concludes that arriving at the recited “a thickness of its conductor circuitry layer being less than a half of the viahole diameter” involves only routine skill in the art and therefore is not patentable.

Claims 25-33 are rejected under 35 U.S.C. §103(a) as being obvious over KINOSHITA in view of U.S. Patent No. 5,744,758 (“TAKENOUCHI”). The Office Action states that KINOSHITA teaches all recitations of claims 25-33 except that it does not disclose that the insulative layer is formed of a composite of thermosetting resin and heat-resistant thermoplastic resin. To make up for this deficiency, the Office Action relies

on a secondary document TAKENOUCHI. The Office Action alleges that TAKENOUCHI, at column 5, line 67 and at column 6, lines 1-5, teaches an insulative layer that is formed of a composite of thermosetting resin and heat-resistant thermoplastic resin. The Office Action concludes that it would have been obvious to combine the above two documents to arrive at claims 25-33 in order to improve electro-conductivity and provide thermal-expansion or contraction rates between materials constituting a multilayer printed wiring board.

Response to Rejections

With respect to the numerous 35 U.S.C. §112 rejections of Claims 1-5, 7, 9-17, 20-23, 25-27 and 31-32. Applicants have amended claims 1-5, 7, 9-14, 16-17, 21-23, 25-27 and 31-32 to address all but one 35 U.S.C. §112 rejections made in the Office Action. As indicated on the Interview Summary, these amendments should overcome the 35 U.S.C. §112 rejections and therefore, the rejections should be withdrawn.

Claim 20 is canceled. Therefore, the rejection to claim 20 is moot.

Applicants respectfully traverse the 35 U.S.C. §112 rejection of claim 15 made on page 3 of the Office Action. As discussed and agreed upon during the personal interview, claim 15, as recited, is clear and definite and therefore, the rejection should be withdrawn.

With respect to rejections to claims 17-23 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,294,744 (“KINOSHITA”), the amended claim 17 recites

that “at least one of the surfaces of the conductor circuits layer is roughened.” As agreed upon by the Examiners during the personal interview, this part of the recitation of the amended claim 17 is not disclosed or suggested by KINOSHITA. Therefore, the 35 U.S.C. §102(e) rejections to claims 17-23 is overcome and should be withdrawn.

With respect to rejections of Claims 1-16 and 24 under 35 U.S.C. §103(a) as being obvious over KINOSHITA, Applicants respectfully submit that the Office Action is mistaken in stating that KINOSHITA shows a viahole having a diameter less than 25 micrometers (column 4, lines 59-61). In fact, in column 4, lines 59-61, the diameters referenced by KINOSHITA is the particle diameters of the inorganic powder of calcium carbonate. Thus it is the particle diameters which are to be below 15 micrometers, not a viahole. Additionally, this document does not suggest or teach that “the thickness of said conductor circuit layer being less than a half of the viahole diameter.” Therefore, this document does not teach or suggest all the recitations of the claimed invention.

The Examiner alleges that modification to KINOSHITA to arrive the particular feature wherein “the thickness of said conductor circuit layer being less than a half of the viahole diameter” is motivated in order to “provide an improvement of finer ultra circuit pattern on the printed wiring board.” While it might be true that one of ordinary skill in the art would like to provide finer ultra circuit patterns, Applicants respectfully submit KINOSHITA does not suggest, explicitly or implicitly, and one of ordinary skill in the art

would not be motivated to provide a thickness of the conductor circuit layer being less than a half of the viahole diameter. Therefore, this rejection should be withdrawn.

With respect to rejections to claims 25-33 under 35 U.S.C. §103(a) as being obvious over KINOSHITA in view of U.S. Patent No. 5,744,758 (“TAKENOUCHI”), Applicants respectfully submit that the understanding of TAKENOUCHI upon which the rejection is based is mistaken. The recited section of TAKENOUCHI in the Office Action, column 5, line 67 and column 6, lines 1-5 does not disclose “an interlaminar insulative layer being formed of a composite of thermosetting resin and heat-resistant thermoplastic resin,” as alleged in the Office Action. Instead, this recited section of TAKENOUCHI discloses a substrate of three layers: thermosetting resin film, metallic layer, and a thermoplastic layer. Obviously, the disclosed substrate of three layers of material is NOT THE SAME as the composite of two materials in the presently claimed invention. Therefore, the combination of the two documents would not arrive at all the recitations of the claimed invention.

Even if the combination were to teach all the recitations of the claimed invention, as the Examiner is fully aware, in order to make a proper combination, there must be some suggestion or motivation in the documents to make such combination. The Examiner alleges that TAKENOUCHI’s composite can be used in order to improve an electro-conductivity and provide thermal-expansion or contraction rates between materials constituting of a multiplayer printed wiring board. However, such motivation is not

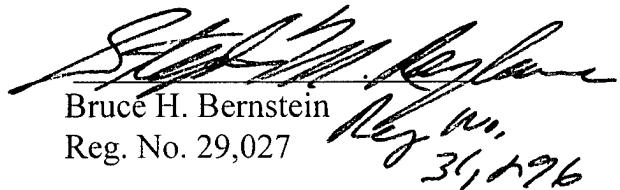
provided in the documents and is not a valid one since TAKENOUCHI does not disclose the use of the composite as discussed above. Therefore, this rejection should also be withdrawn.

Moreover, even if the documents were properly combinable, the claimed invention still would not result. In this regard, there is absolutely no teaching or suggestion in TAKENOUCHI to provide a printed wiring board claimed parameters. Accordingly, the rejection should be withdrawn.

CONCLUSION

In view of the foregoing, it is believed that all of the claims in this application are in condition for allowance, which action is respectfully requested. If any issues yet remain which can be resolved by a telephone conference, the Examiner is respectfully invited to telephone the undersigned at the telephone number below.

Respectfully submitted,
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October 24, 2002
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Appendix: Marked up copy of the amendments.

1. A multilayer printed wiring board [having] comprising conductor [circuitry] circuit layers having a thickness and a surface and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having [formed through them holes each] through-holes having an inner wall filled with a plating layer having a surface to form a viahole having a diameter, [characterized by] wherein:
the surface of said plating layer [exposed] extending out of the [hole for the viahole being formed substantially flat] through-holes and lying in a substantially same level as the surface of the conductor circuit layer disposed in the interlaminar insulative resin layer in which the plating layer also lies; and
the thickness of said conductor [circuitry] circuit layer being less than a half of the viahole diameter.
2. The multilayer printed wiring board as set forth in Claim 1, wherein the inner wall of the [hole] through-hole is roughened.
3. The multilayer printed wiring board as set forth in Claim 1, wherein the plating layer surface and conductor circuit layer [exposed] extending out of the [hole] through-holes are roughened.
4. The multilayer printed wiring board as set forth in Claim 1, wherein at least

one of the surfaces of the [inner] conductor circuits [connected to each other by the viahole]
are roughened.

5. The multilayer printed wiring board as set forth in Claim 1, wherein a further viahole is formed [on] in the viahole.

7. The multilayer printed wiring board as set forth in Claim 1, wherein [the] a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4.

8. The multilayer printed wiring board as set forth in Claim 1, wherein the conductor [circuitry] circuit layer has a thickness less than 25 μm .

9. A multilayer printed wiring board [having] comprising conductor [circuitry] circuit layers having a thickness and a surface and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having [formed through them holes each] through-holes having an inner wall filled with a plating layer having at least one surface to form a viahole having a diameter, [characterized in that] wherein the thickness of said conductor [circuitry] circuit layer is less than a half of the viahole diameter and less than 25 μm .

10. The multilayer printed wiring board as set forth in Claim 9, wherein the inner wall of the [hole] through-holes is roughened.

11. The multilayer printed wiring board as set forth in Claim 9, wherein a

depression is formed on [the] a central surface portion of the plating layer surface [exposed out of the hole for] extending out of the [viahole] through-holes.

12. The multilayer printed wiring board as set forth in Claim 9, wherein the surface of the plating layer [surface] and the surface of the conductor circuit [surface] layer [exposed out of the hole for the] extending out of the [viahole] through-holes are roughened.

13. The multilayer printed wiring board as set forth in Claim 9, wherein at least one of the surfaces of the [inner] conductor circuit layer [circuits connected to each other by the viahole are] is roughened.

14. The multilayer printed wiring board as set forth in Claim 9, wherein a further viahole is formed [on] in the viahole.

16. The multilayer printed wiring board as set forth in Claim 9, wherein [the] a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4.

17. A multilayer printed wiring board [having] comprising conductor [circuitry] circuit layers each with at least one surface wherein at least one of the surfaces of the conductor circuit layer is roughened and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having [formed through then holes each] through-holes, having an inner wall wherein the inner wall is

roughened, filled with a plating layer to form a viahole, [characterized by] wherein:

[said hole having an inner wall thereof roughened;]

 said roughened inner wall [being] is covered with a roughened electroless plating layer; and

 an inner space of said [hole] through-hole defined by the electroless plating layer and is filled with an electroplating layer.

18. The multilayer printed wiring board as set forth in Claim 17, wherein depressions are formed in the central surface portion of the plating layer surface [exposed] extending out of the [hole for the viahole] through-holes.

19. The multilayer printed wiring board as set forth in Claim 17, wherein the plating layer surface and conductor circuit surface [exposed] extending out of the [hole for the viahole] through-holes are roughened.

21. The multilayer printed wiring board as set forth in Claim 17, wherein a further viahole is formed [on] in the viahole.

23. The multilayer printed wiring board as set forth in Claim 17, wherein [the] a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4.

24. The multilayer printed wiring board as set forth in Claim 17, wherein the conductor [circuitry] circuit layer has a thickness less than 25 μm .

25. A multilayer printed wiring board [having] comprising conductor [circuitry] circuit layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having [formed through them holes each] through-holes, having an inner wall, filled with a plating layer to form a viahole, [characterized by:]

 said interlaminar insulative resin [layer] layers being formed from a composite of fluororesin and heat-resistant thermoplastic resin, composite of fluororesin and thermosetting resin, or a composite of thermosetting resin and heat-resistant thermoplastic resin.

26. The multilayer printed wiring board as set forth in Claim 25, wherein the interlaminar insulative resin layer is made of a composite of fluororesin fiber cloth, wherein said cloth comprises voids, and wherein thermosetting resin is impregnated in the voids in the cloth.

27. The multilayer printed wiring board as set forth in Claim 25, wherein the inner wall of the [hole] through-holes is roughened.

28. The multilayer printed wiring board as set forth in Claim 25, wherein depressions are formed in the central surface portion of the plating layer surface [exposed] extending out of the [hole for the viahole] through-holes.

29. The multilayer printed wiring board as set forth in Claim 25, wherein the plating layer surface and conductor circuit surface [exposed] extending out of the [hole for the viahole] through-holes are roughened.

31. The multilayer printed wiring board as set forth in Claim 25, wherein a further viahole is formed [on] in the viahole.

32. The multilayer printed wiring board as set forth in Claim 25, wherein [the] a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4.

33. The multilayer printed wiring board as set forth in Claim 25, wherein the conductor [circuitry] circuit layer has a thickness less than 25 μm .